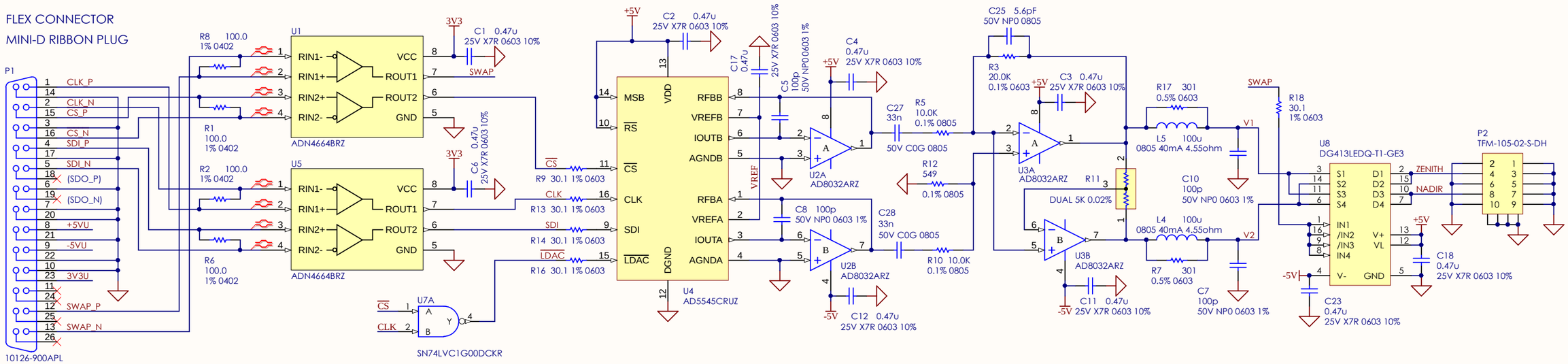
COPYRIGHT 2018 CALIFORNIA INSTITUTE OF TECHNOLOGY. GOVERNMENT SPONSORSHIP ACKNOWLEDGED.

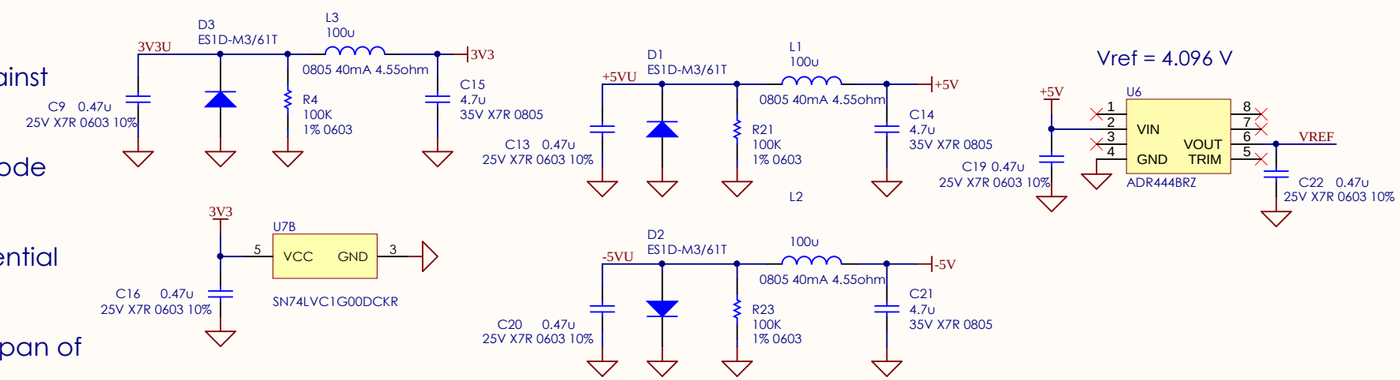
REVISION HISTORY

REV	DESCRIPTION	CAT	DWN	ENGR	
A	---------- INITIAL RELEASE ----------	II			SEE JPL DATA MANAGMENT SYSTEM FOR APPROVAL SIGNATURES AND DATES
B	UPDATED VARIOUS PARTS. ADDED GUARD RING AND ROGERS 4350B.	II			
C	ADDED OUTPUT SWITCH CHANNGED U1 TO DUAL, AND ADDED SWAP INPUT.	II			



NOTES

1. Place grounded guard trace around node [U3-6, R11-3], guarding against U3-7 node and U3-1 node.
2. Zero offset of height measurement is 19.5mm *k, where k = common-mode voltage / differential voltage
3. Resistor values shown give k in the range - 0.025 to +0.025, with a differential drive level of 0.5 of max. This gives a zero offset span of +/- 0.5 mm.
4. Reducing the differential drive level to 0.05 of max gives a zero offset span of +/- 5mm, with a proportional reduction in S/N.



10369690	MIT
NEXT ASSEMBLY	USED ON
APPLICATION	

DO NOT SCALE DRAWING
INTERPRET DEMENSIONING AND TOLERANCING PER ASME Y14.5 2009
INTERPRET DWG PER ASME Y14.100

CONTRACT NO _____

DWN	C SHELTON
ENGR	C SHELTON

SEE JPL DATA MANAGEMENT SYSTEM FOR APPROVAL SIGNATURES AND DATES

JET PROPULSION LABORATORY

CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CA 91109

TITLE
SCHEMATIC DIAGRAM,
EDGE SENSOR DRIVE BOARD
- MATRIX V5

SIZE	DAI	DWG NO	REV
B	23835	10369688	C

SCALE: 1/1 | UNCLASSIFIED | SHEET 1 OF 1

ALTIUM GENERATED

REV 05/2018

JPL_B_SH1