Sensor Control FPGA
sensor cntrl_FPGA.SchDoc

Sensor Control DRIVE
sensor cntrl_DRIVE.SchDoc

Sensor Control SENSE
sensor cntrl_SENSE.SchDoc

Sensor Control Power Supplies
sensor cntrl_POWER.SchDoc

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DRIVE_CLK
DRIVE_CSR
DRIVE_SDI
DRIVE_PSYNC
DRIVE_SWAP_N
DRIVE_SWAP_Z

SENSE_SCK
SENSE_CNV
SENSE_SDO

ENV_VDD
ENV_RH
ENV_T

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SEE JPL DATA MANAGEMENT SYSTEM FOR APPROVAL
SIGNATURES AND DATES

JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
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REVISION HISTORY

REV DESCRIPTION
A INITIAL RELEASE

CONTRACT NO.

10398567 TMT

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A 23835 10398566
PIO01-03 are used internally in the CMOD A7.

Socket for CMOD A7 Artix-7 Module
48-pin DIP 0.600 inch row spacing

Command and Control Connection from Edge Sensor Interface Board
NOTES

Notes on the isolated power part (DCR010505U, above):
- Place the split between the isolated ground plane and the main ground plane under this part.
- Minimize total capacitance of node connecting to SYNC pin and keep on one layer.
- Place guard ring around node connecting to SYNC pin and connect it to -VS pins.
- This part has a 150°C internal thermal cutout which auto-resets at 130°C.
- The VREC pin does not otherwise have intrinsic current limiting, while the +V_OUT pin has current limiting and can be short-circuited indefinitely.

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