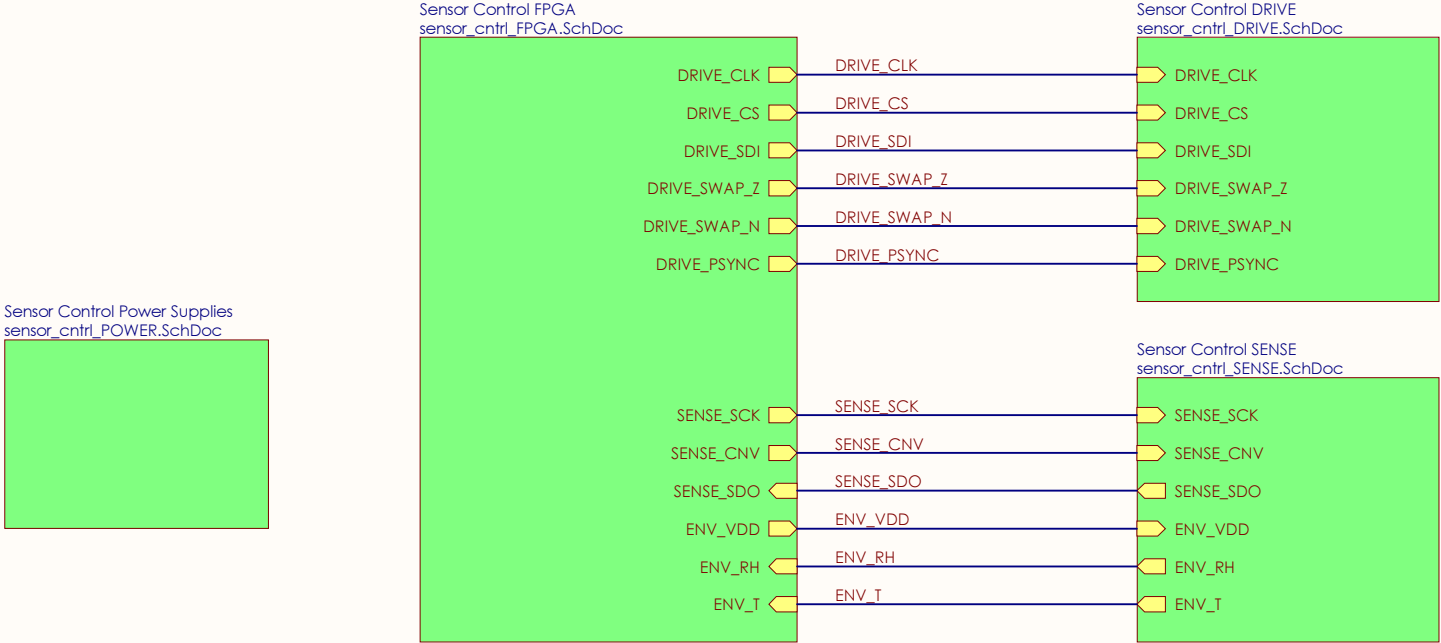


REVISION HISTORY					
REV	DESCRIPTION	CAT	DWN	ENGR	SEE JPL DATA MANAGEMENT SYSTEM FOR APPROVAL SIGNATURES AND DATES
A	----- INITIAL RELEASE -----	II	-	-	



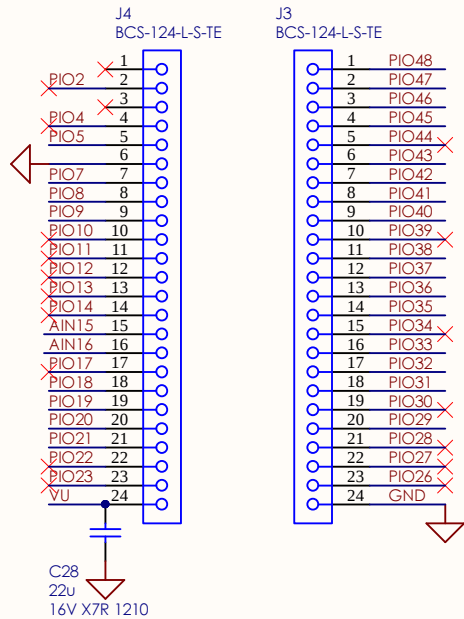
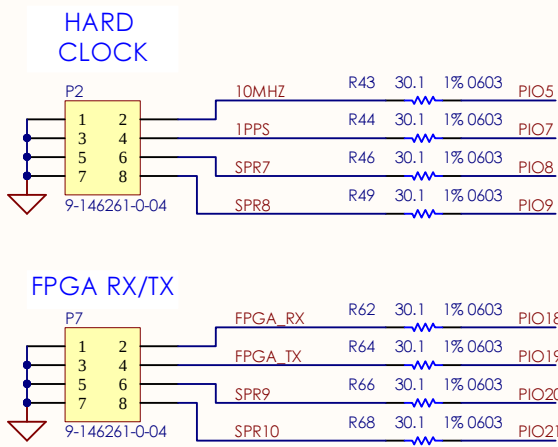
		CONTRACT NO _____		JET PROPULSION LABORATORY			
				CALIFORNIA INSTITUTE OF TECHNOLOGY PASADENA, CA 91109			
		DWN	C SHELTON	TITLE SCHEMATIC DIAGRAM, EDGE SENSOR CONTROLLER			
		ENGR	C SHELTON				
		SEE JPL DATA MANAGEMENT SYSTEM FOR APPROVAL SIGNATURES AND DATES		SIZE DAI DWG NO REV B 23835 10398566 A			
10398567	TMT						
NEXT ASSEMBLY	USED ON						
APPLICATION				SCALE: NONE UNCLASSIFIED		SHEET 1 OF 5	

NOTES: UNLESS OTHERWISE SPECIFIED

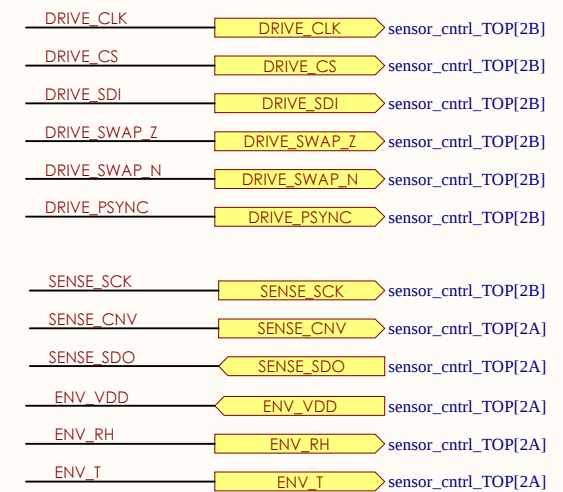
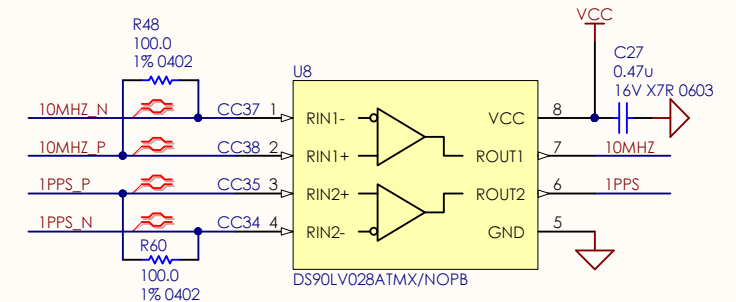
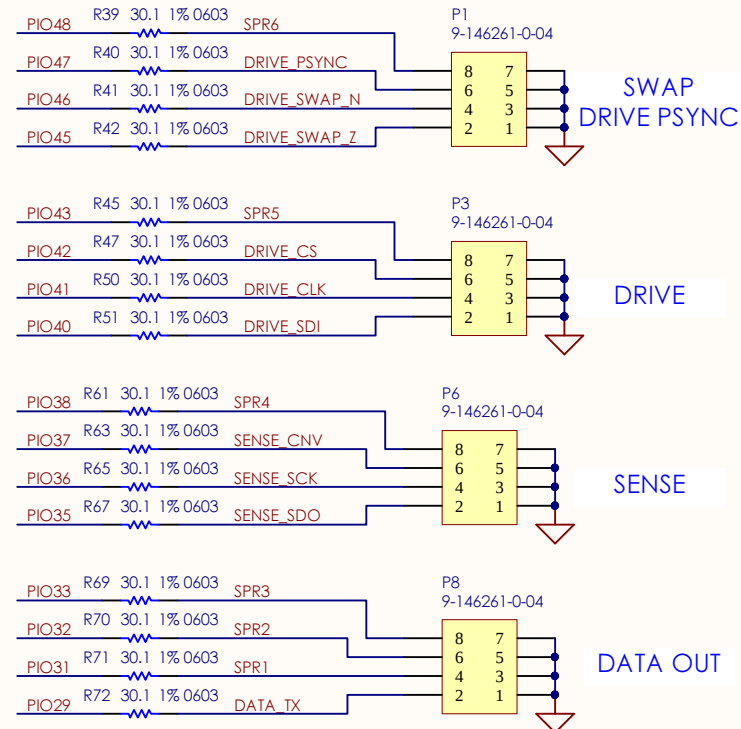
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GOVERNMENT SPONSORSHIP ACKNOWLEDGED.

DO NOT SCALE DRAWING
INTERPRET DIMENSIONING AND
TOLERANCING PER ASME Y14.5 2009
INTERPRET DWG PER ASME Y14.100

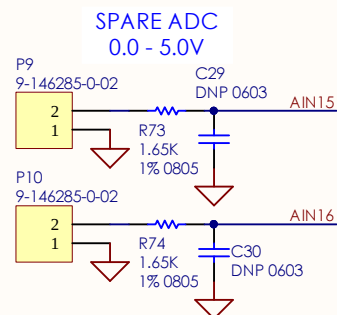
PIO-01,-03 are used internally in the CMOD A7.



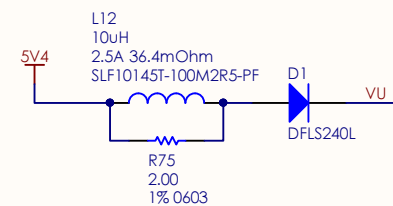
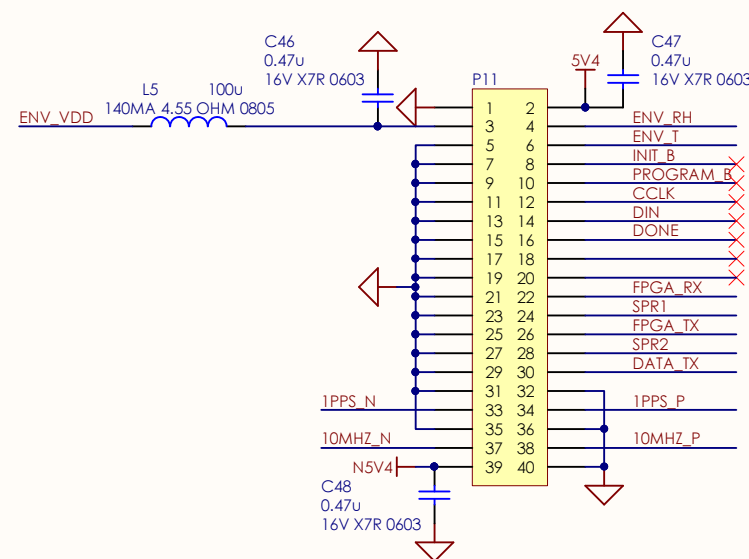
Socket for CMOD A7 Artix-7 Module
48-pin DIP 0.600 inch row spacing

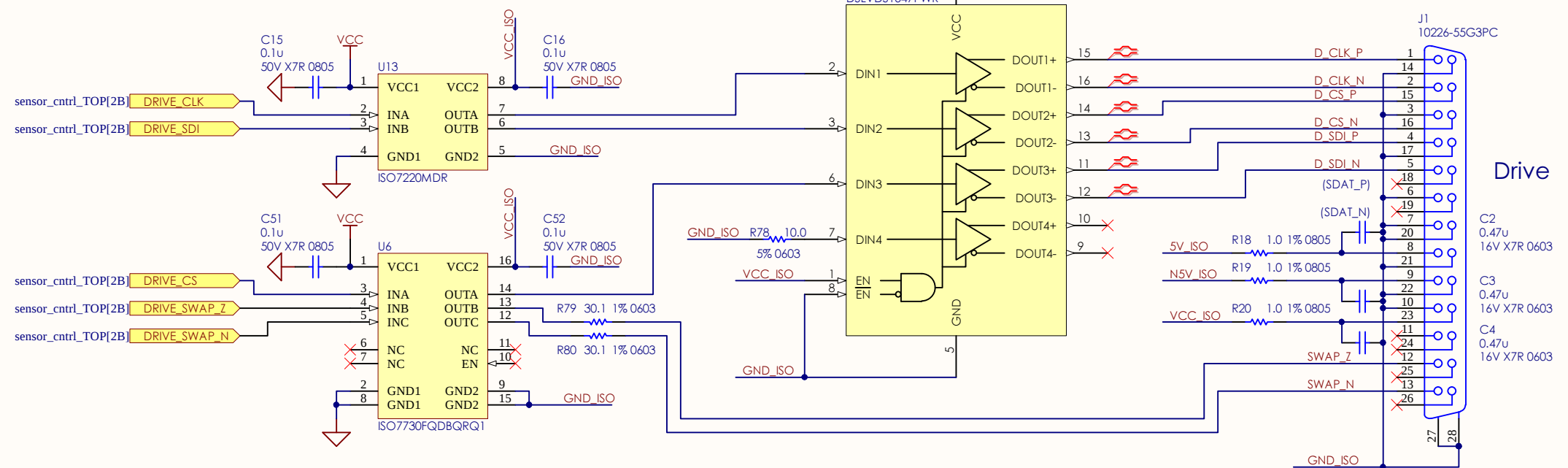
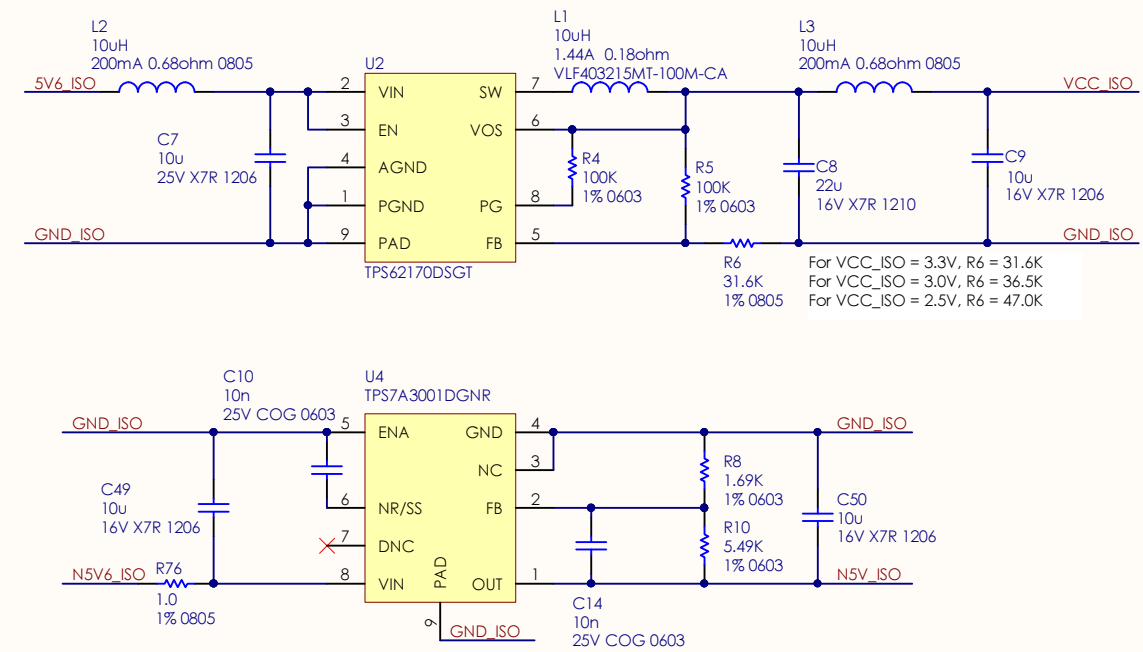
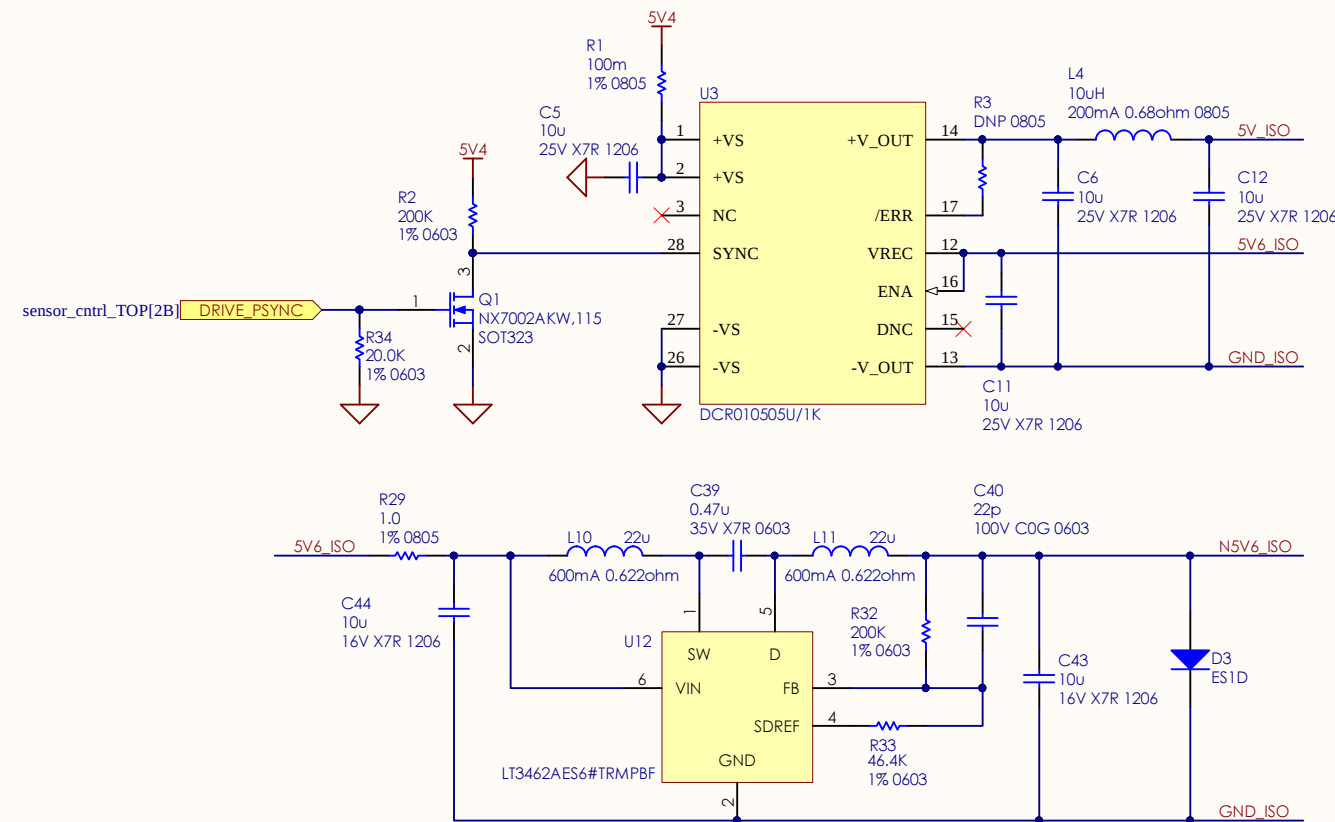


FPGA



Command and Control Connection
from Edge Sensor Interface Board





NOTES

Notes on the isolated power part (DCR010505U, above):

Place the split between the isolated ground plane and the main ground plane under this part.

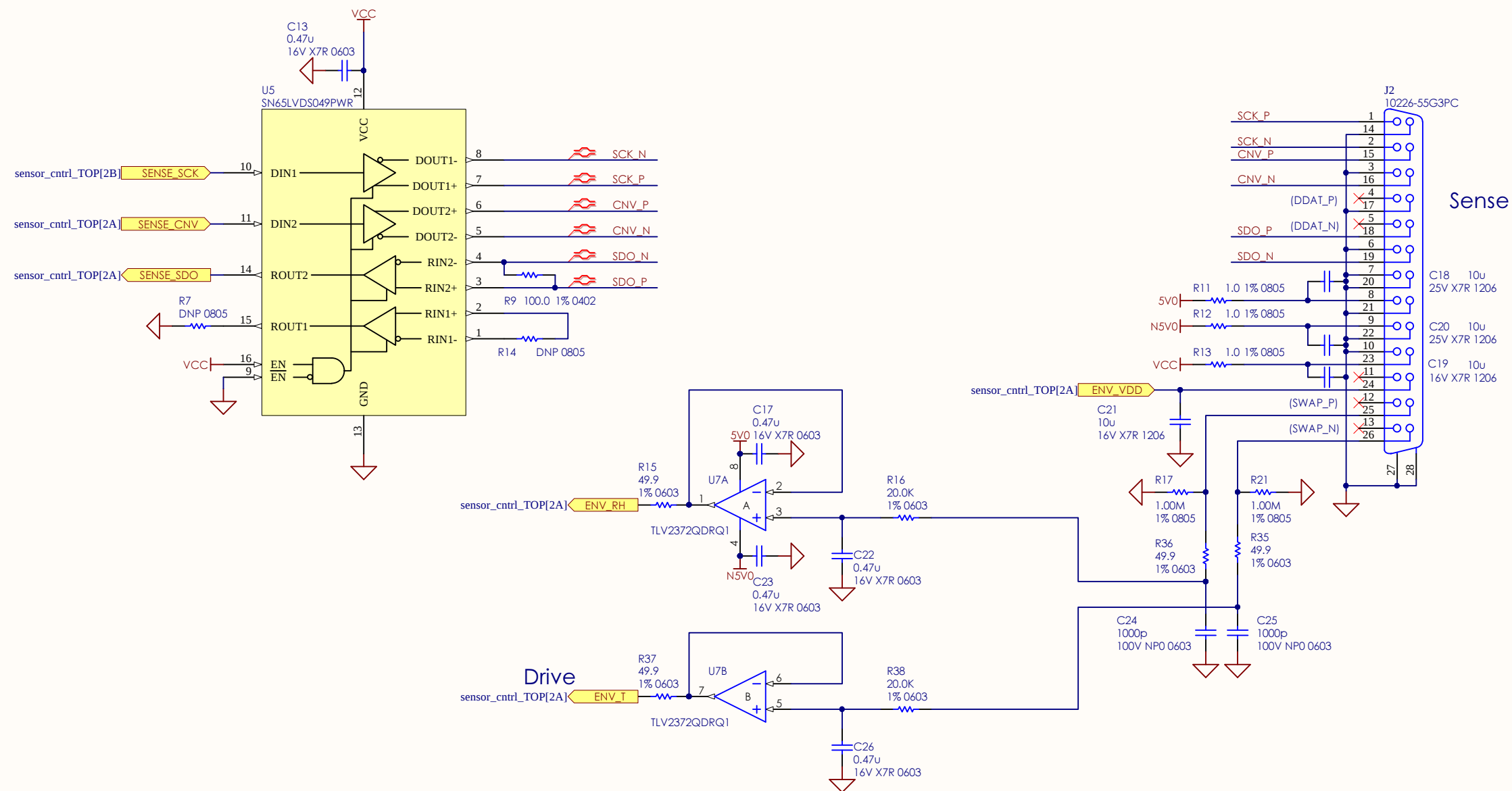
Minimize total capacitance of node connecting to SYNC pin and keep on one layer.

Place guard ring around node connecting to SYNC pin and connect it to -VS pins.

This part has a 150C internal thermal cutout which auto-resets at 130C.

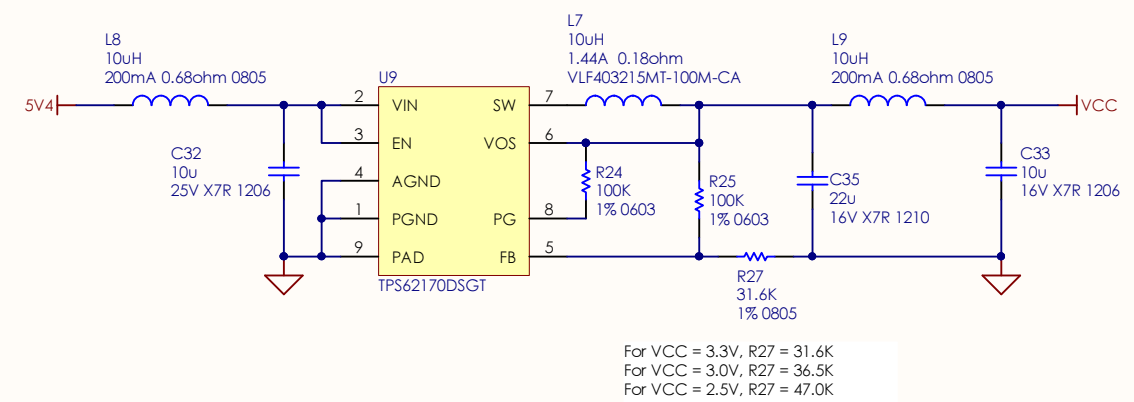
The VREC pin does not otherwise have intrinsic current limiting, while the +V_OUT pin has current limiting and can be short-circuited indefinitely.

DRIVE INTERFACE



SENSE INTERFACE

SEE SHEET 1 FOR EXPORT COMPLIANCE STATEMENT AND/OR PROPRIETARY INFORMATION	SIZE B	DAI 23835	DWG NO 10398566	REV A
	SCALE:	NONE	UNCLASSIFIED	SHEET 4 OF 5



JPL B SH2