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REVISION HISTORY					
REV	DESCRIPTION	CAT	DWN	ENGR	SEE JPL DATA MANAGEMENT SYSTEM FOR APPROVAL SIGNATURES AND DATES
A	_____ INITIAL RELEASE _____	II	-	-	
B	CORRECTED R79 & R97. PREPARED FOR UNLIMITED RELEASE.	II	C. SHELTON	C. SHELTON	
C	CHANGE FROM CONCERTO TO DELFINO SUPPORT. ADDED DIFFERENTIAL CURRENT SENSE AND ENCODER OPTIONS.	II	C. SHELTON	C. SHELTON	
D	CHANGED FORM FACTOR. ADDED MCU DIRECTLY TO BOARD. REMOVED ANALOG ENCODER. REMOVED 18-BIT ADC. UPDATED CONNECTORS. ADDED TEMPERATURE/HUMIDITY SENSOR AND 1-WIRE ID CONNECTOR. UPDATED CURRENT-SENSE COMPONENTS.	II	C. SHELTON	C. SHELTON	

Sheet Listing

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Title page and contents

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Microcontroller GPIO and Memory

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Microcontroller Support

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Microcontroller Power

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VC, Offload & Snubber Hall Sensors

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Voice Coil Driver

12

Offload Motor Driver

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Snubber Motor Driver

4. DIAGNOSTIC (AUX) HEADERS MATE WITH SAMTEC TCSD, 2mm PITCH, CABLE ASSEMBLIES.
3. PLACE GND1, GND2, AND GND 3 ON THE FRONT OF THE BOARD NEAR THE EDGES. PLACE GND4, GND5, AND GND6 ON THE REAR SIDE, OPPOSITE THE GNDs ON THE FRONT. LABEL EACH INSTANCE ON THE SILKSCREEN WITH "GND".
2. ALL CAPACITORS ARE 20% TOLERANCE.
1. ALL RESISTORS ARE 1% TOLERANCE.

NOTES: UNLESS OTHERWISE SPECIFIED

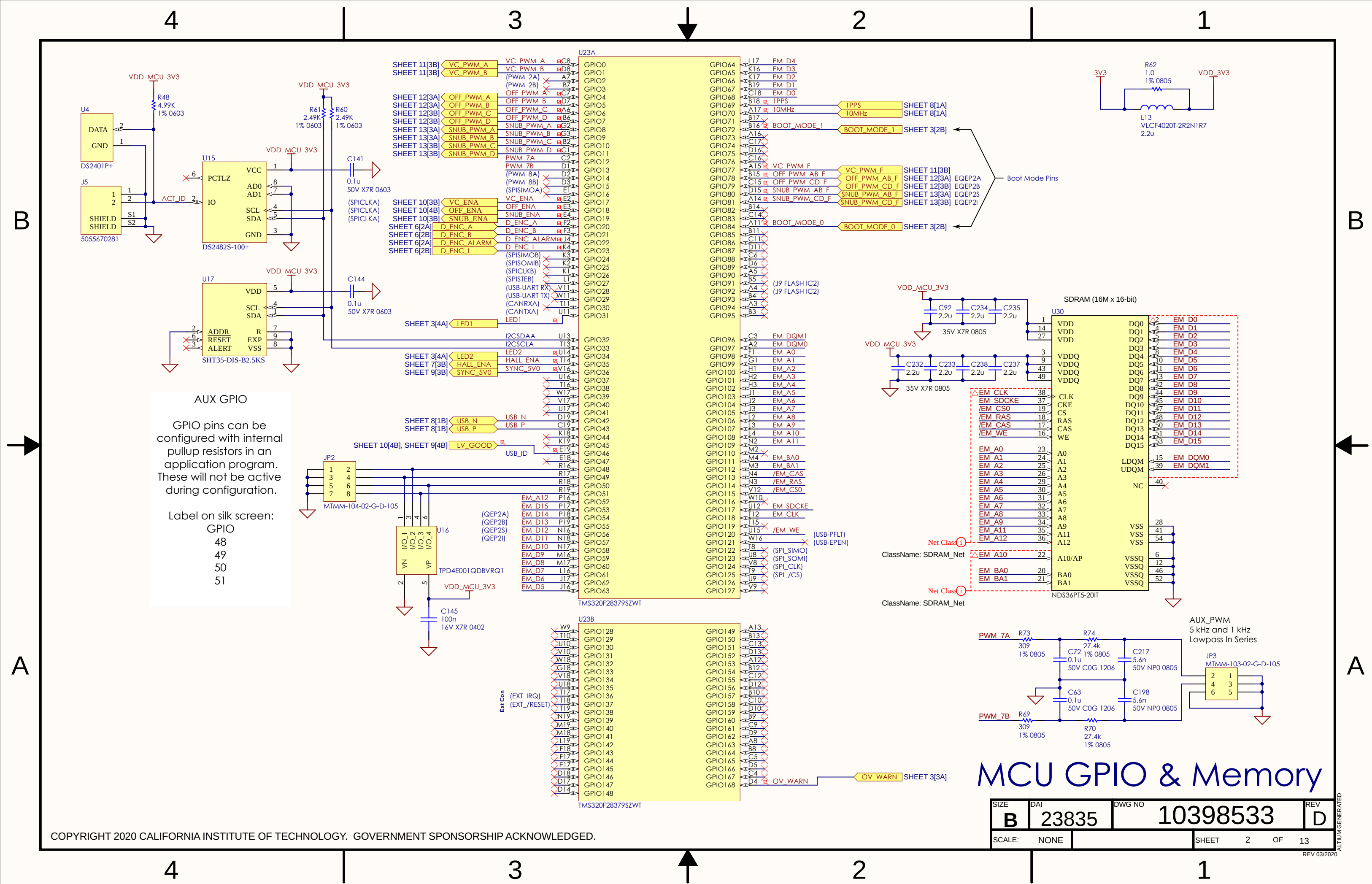
DO NOT SCALE DRAWING
INTERPRET DEMENSIONING AND
TOLERANCING PER ASME Y14.5 2009
INTERPRET DWG PER ASME Y14.100

		CONTRACT NO _____	
		DWN	C. SHELTON
		ENGR	C. SHELTON
		SEE JPL DATA MANAGEMENT SYSTEM FOR APPROVAL SIGNATURES AND DATES	
10398534	TMT		
NEXT ASSEMBLY	USED ON		
APPLICATION			

JET PROPULSION LABORATORY			
CALIFORNIA INSTITUTE OF TECHNOLOGY PASADENA, CA 91109			
TITLE SCHEMATIC DIAGRAM, M1 ACTUATOR DRIVER			
SIZE B	DAI 23835	DWG NO 10398533	REV D
SCALE: NONE		SHEET 1 OF 13	

ALTUM GENERATED

REV 05/2018



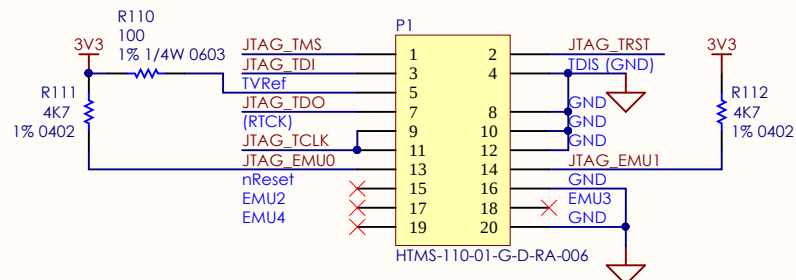
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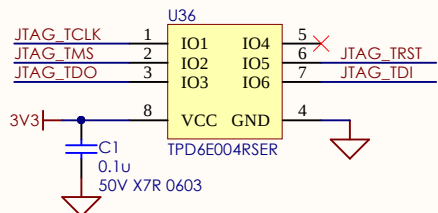
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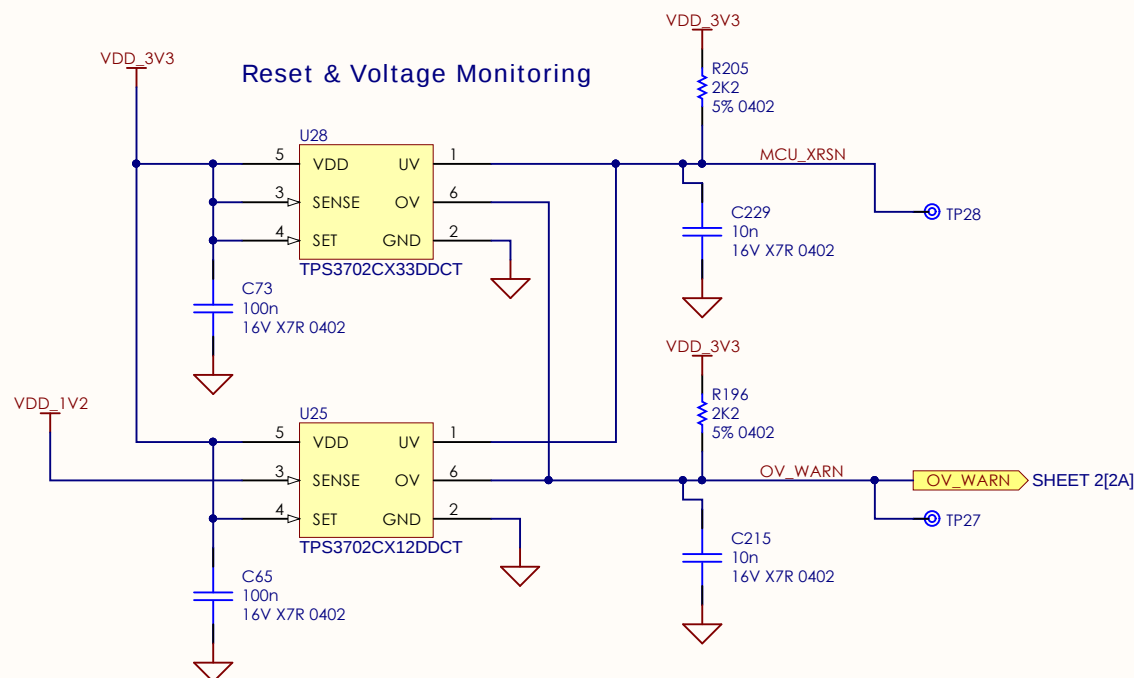
EMULATOR CONNECTOR



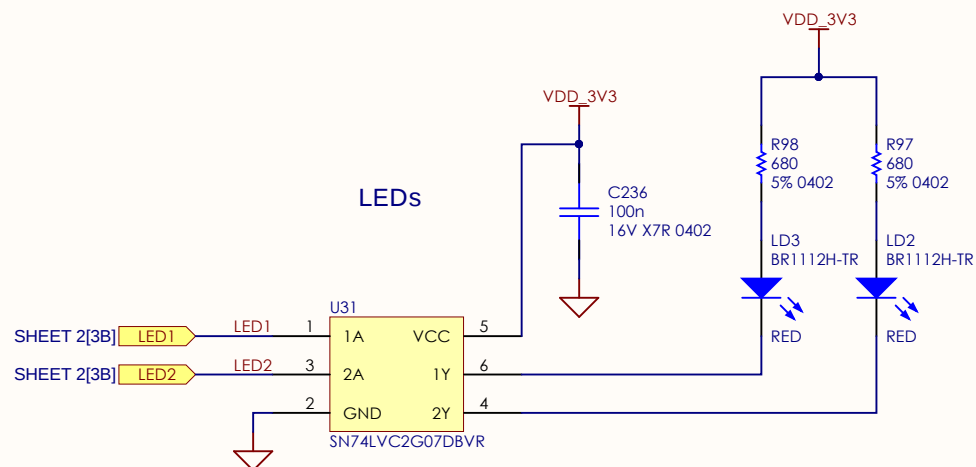
USE SULLINSSFH41-PPPB-D10-ID-BK AS PROTECTIVE CAP



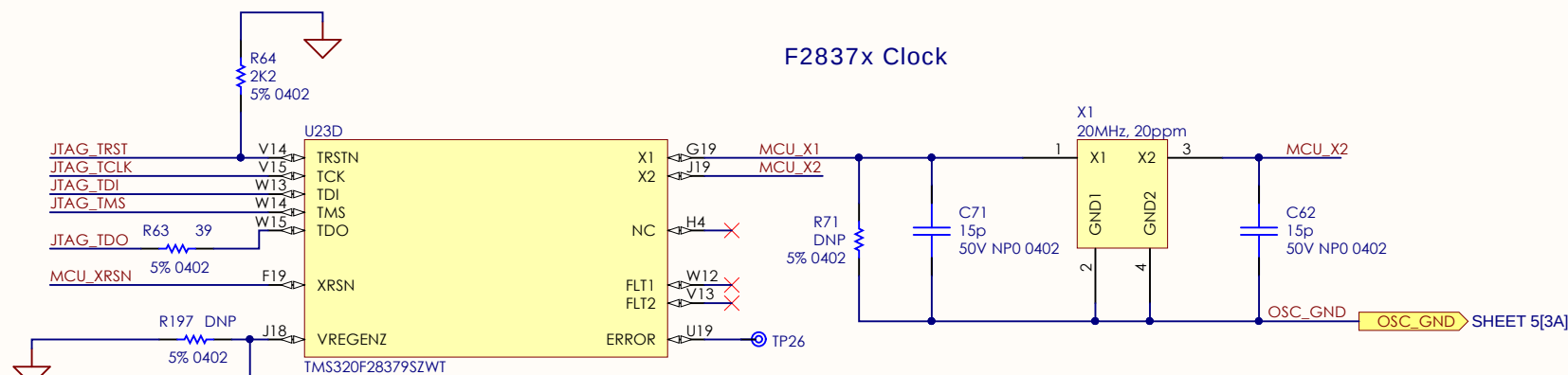
Reset & Voltage Monitoring



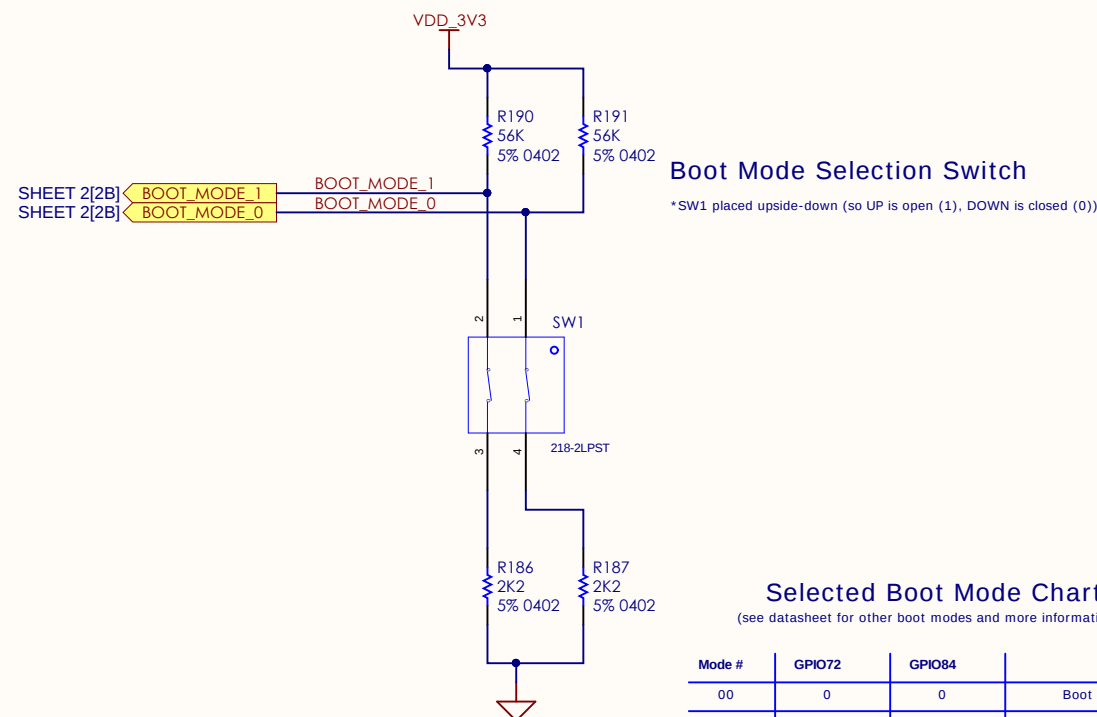
LEDs



F2837x Clock



Boot Mode Selection Switch

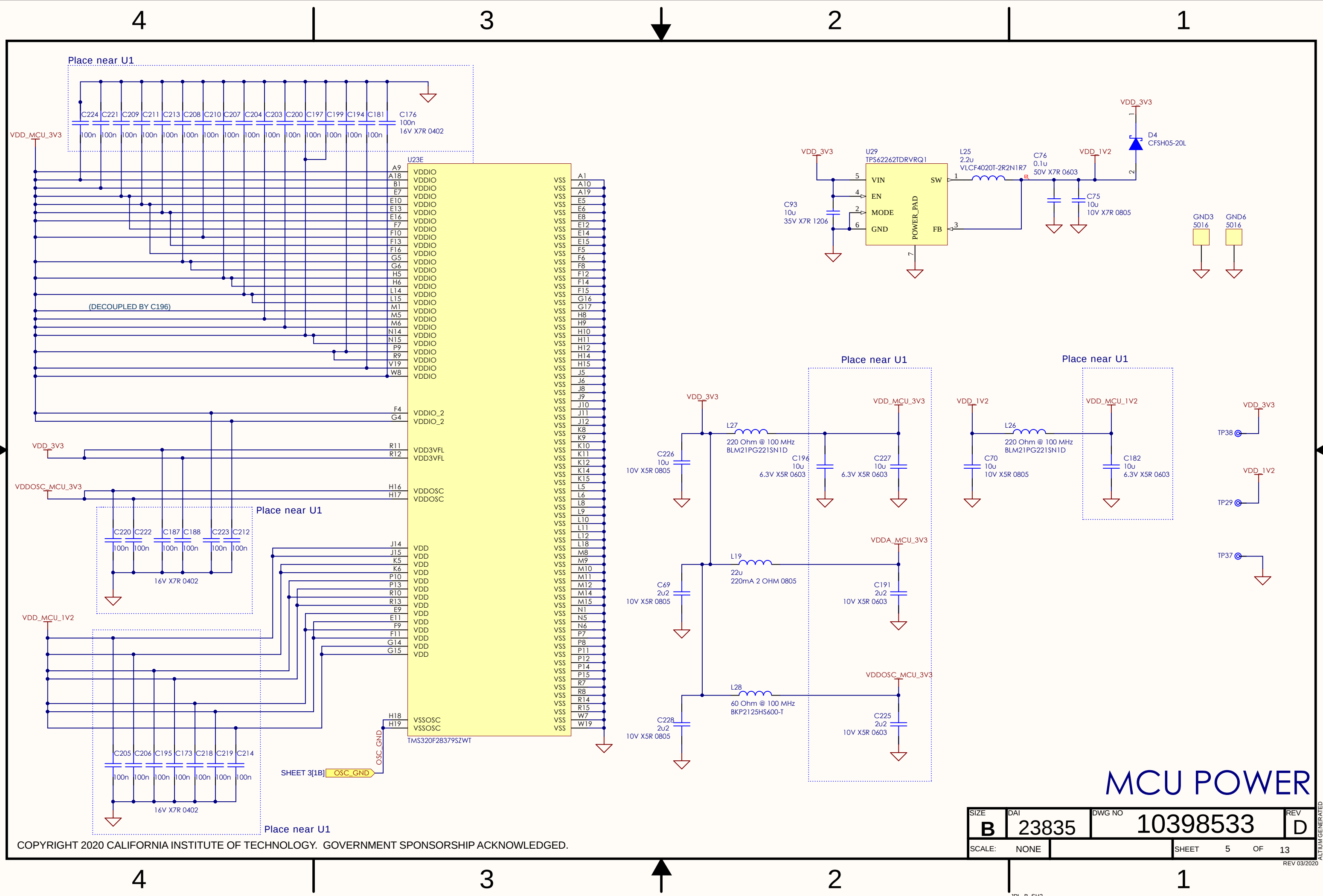


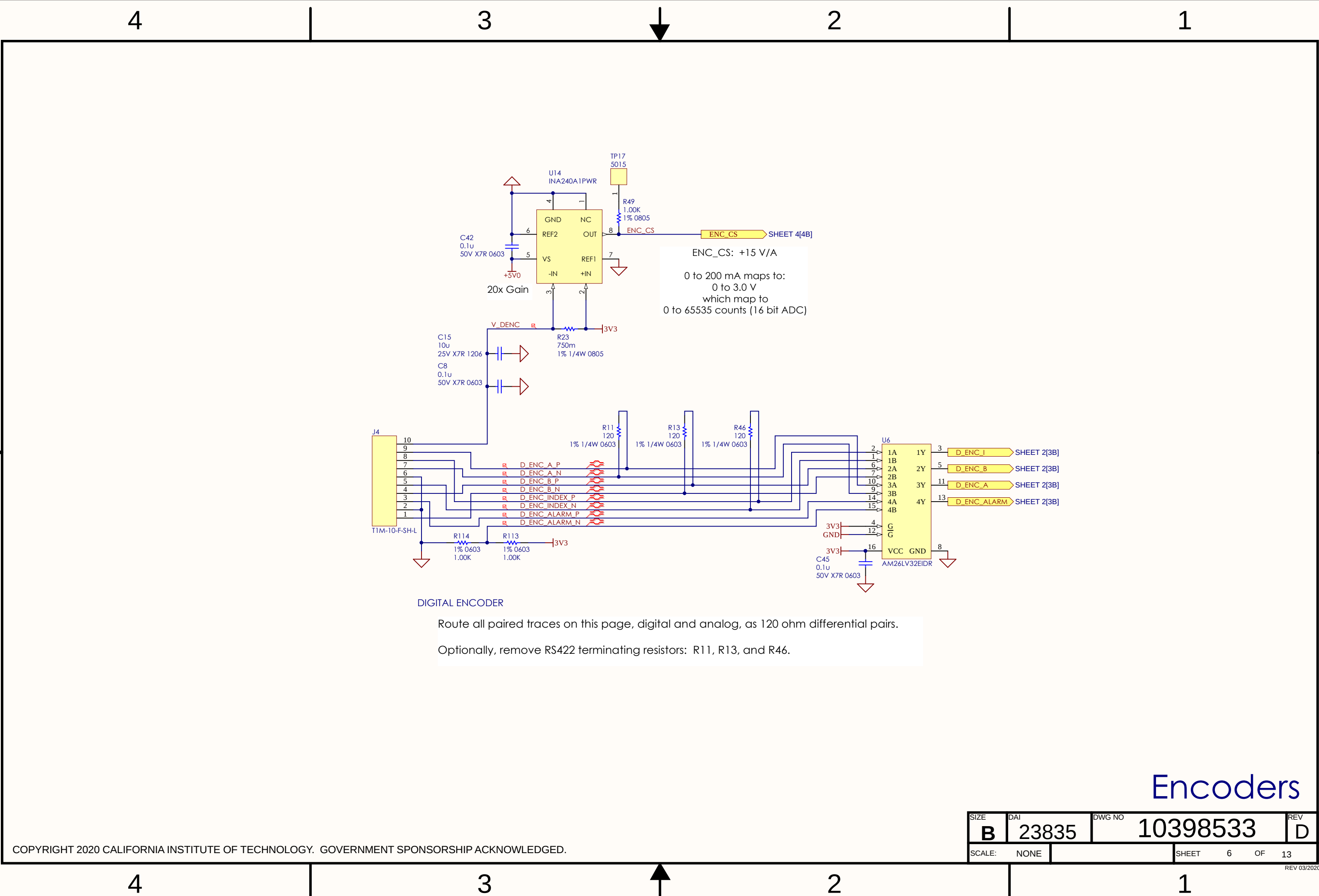
Selected Boot Mode Chart

(see datasheet for other boot modes and more information)

Mode #	GPIO72	GPIO84	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI
02	1	0	Wait Boot Mode
03	1	1	Get Mode (Flash by default)

MCU SUPPORT



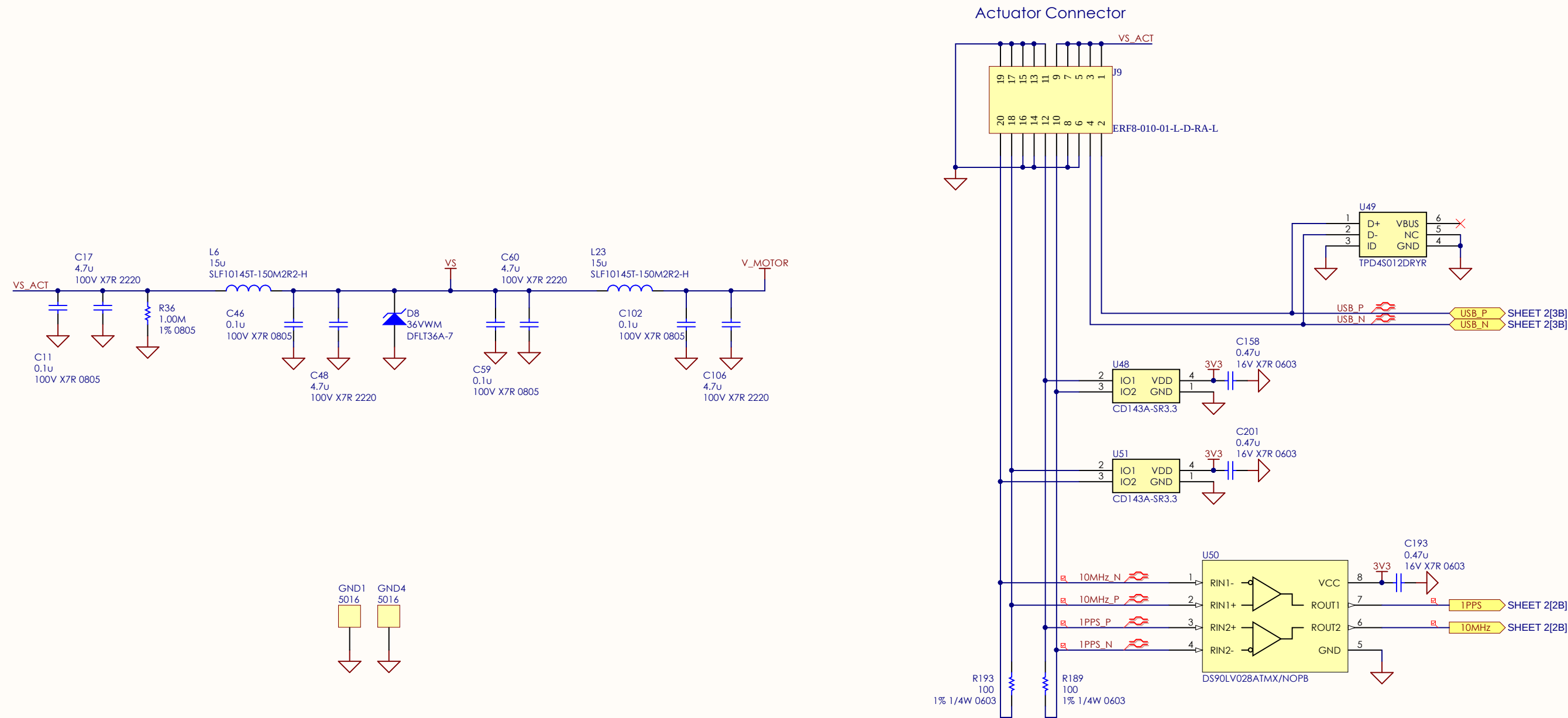


B

B

A

A



Comm and Power I/O

SIZE	DAI	DWG NO	REV
B	23835	10398533	D
SCALE:	NONE	SHEET 8 OF 13	

4

3

2

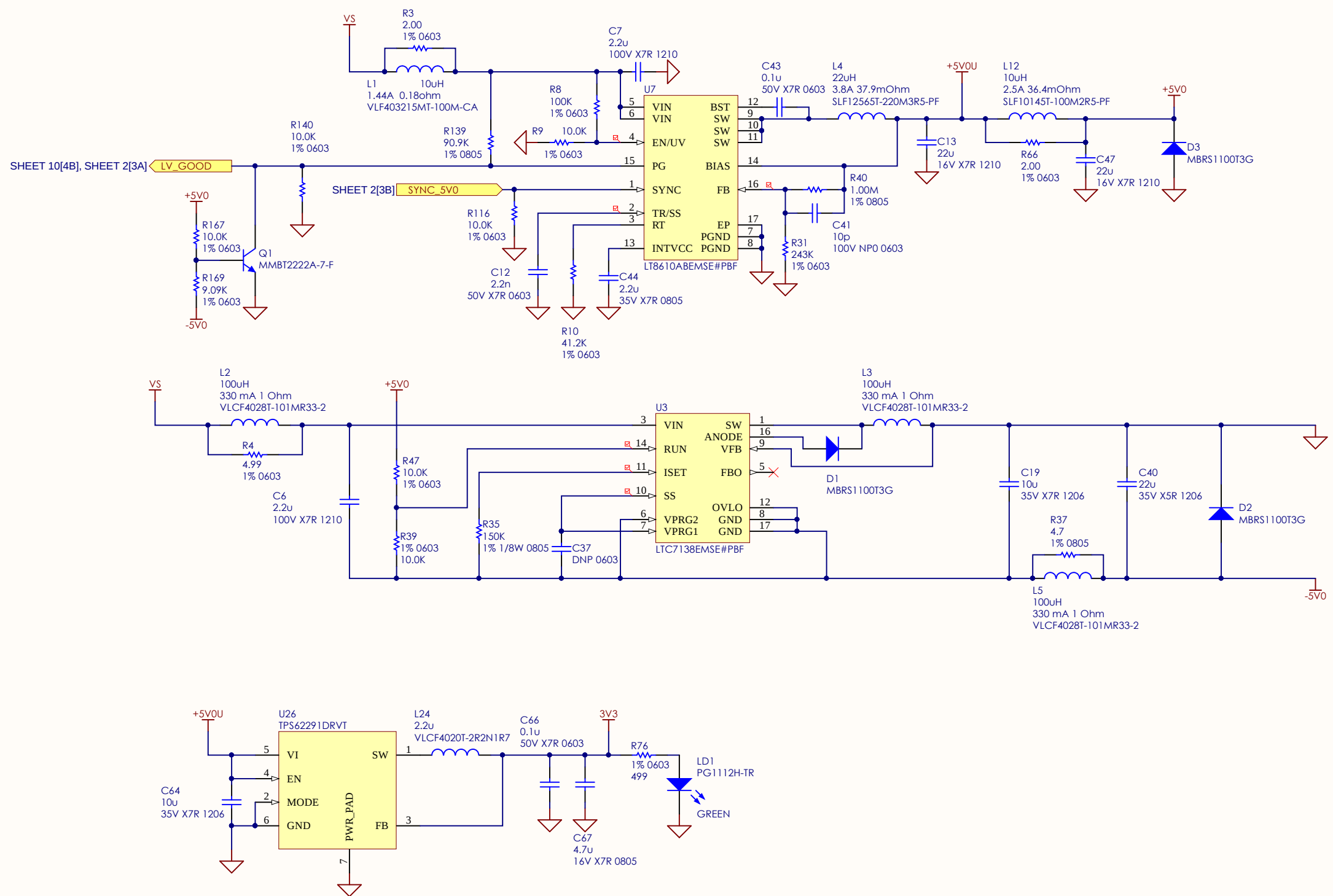
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B

B

A

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Fixed Power Supplies

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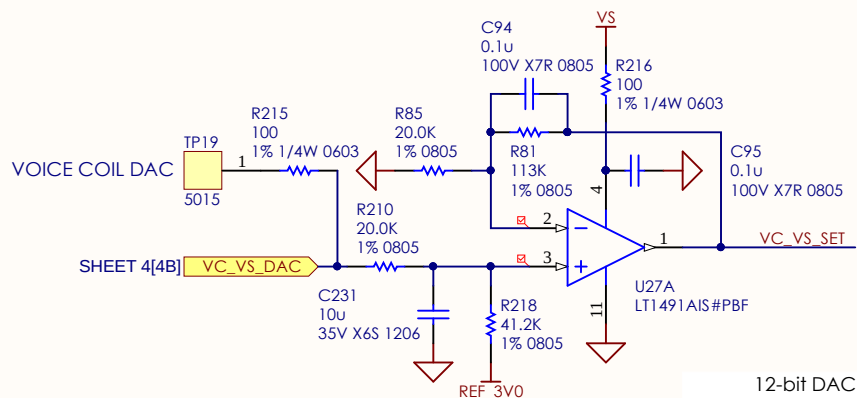
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B	23835	10398533	D
SCALE:	NONE	SHEET 9 OF 13	

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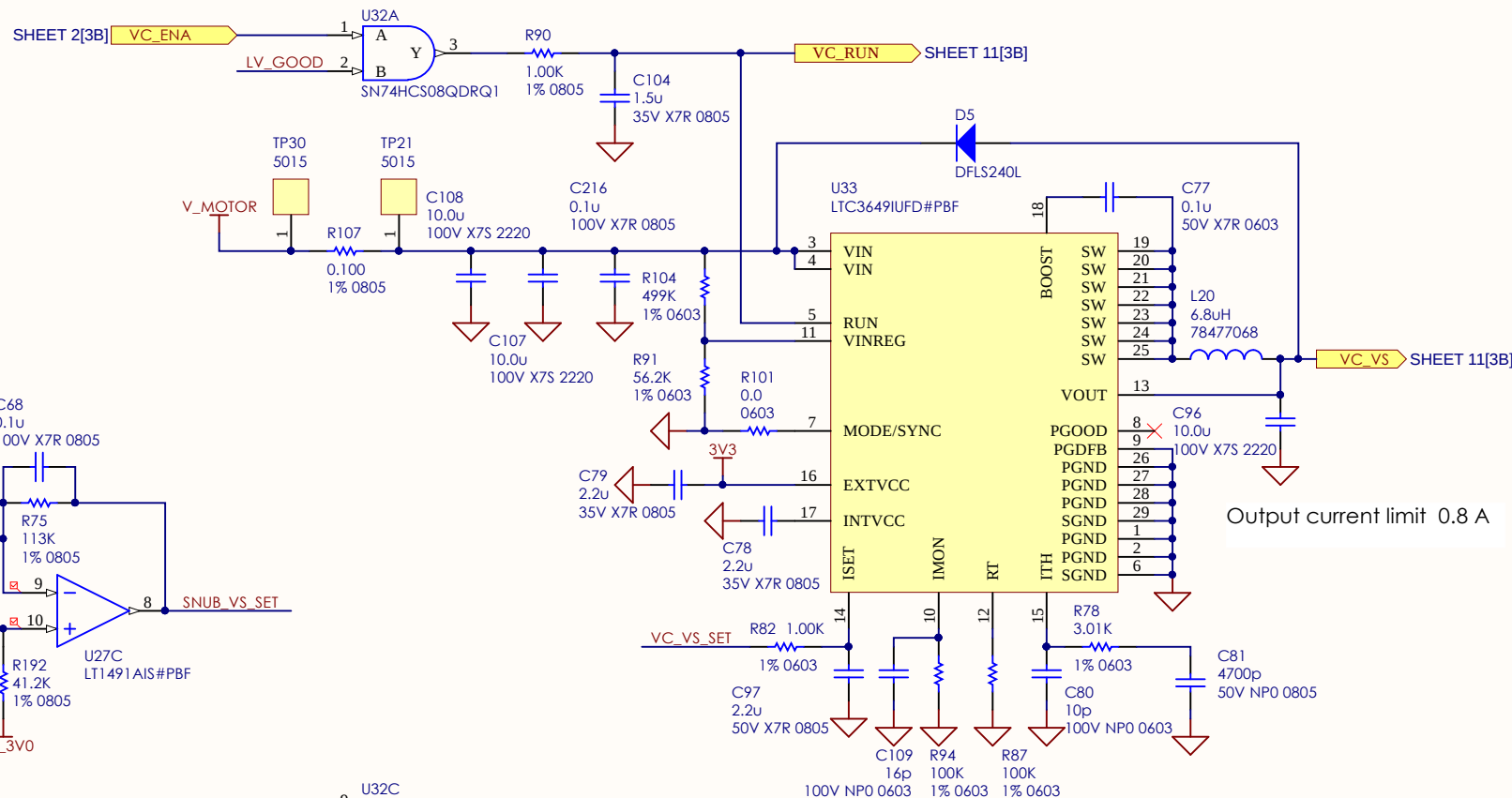
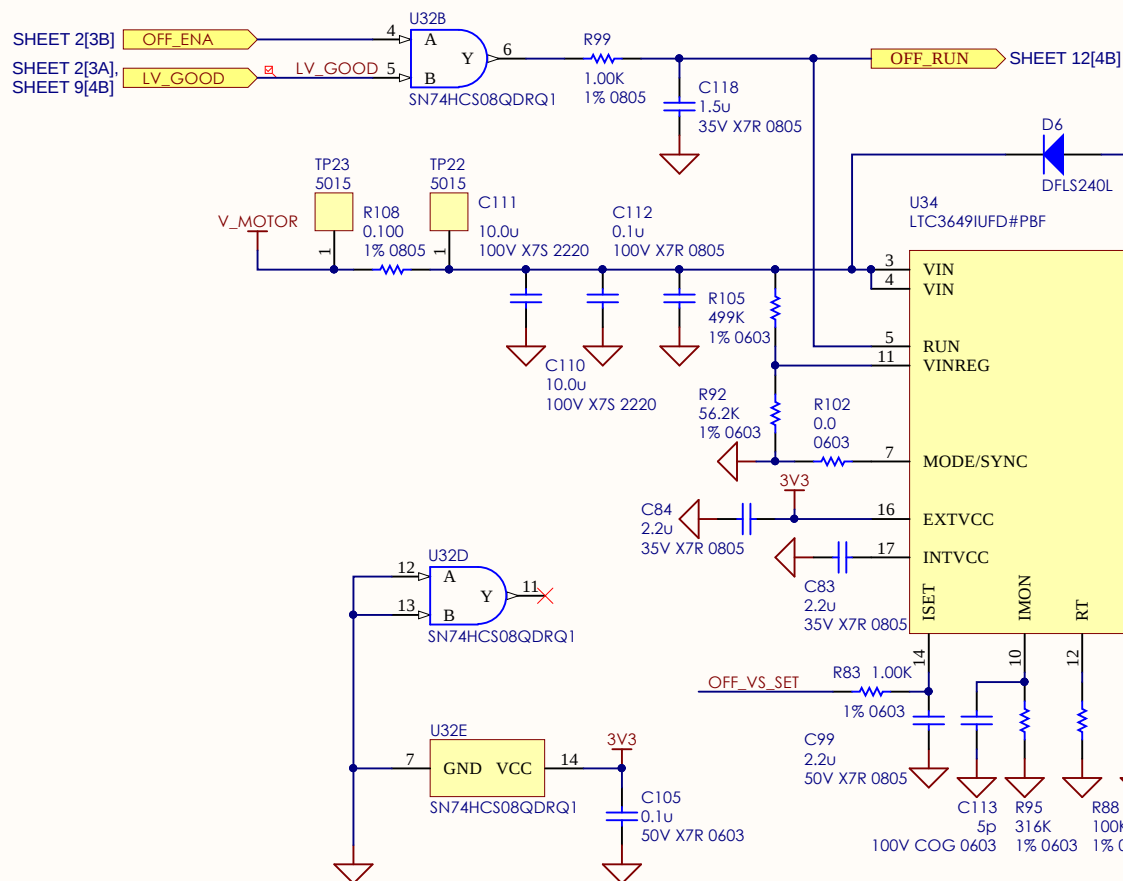
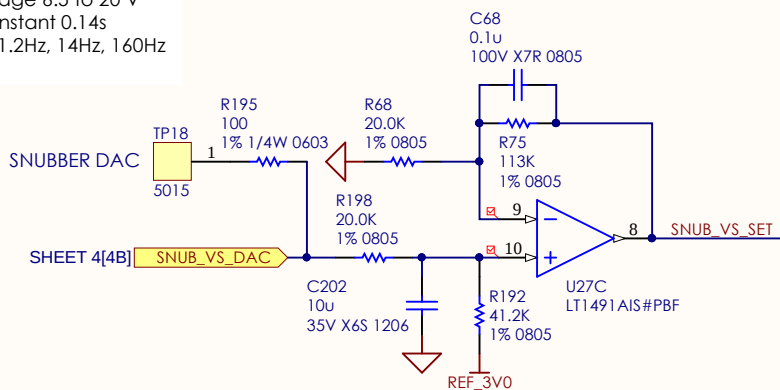
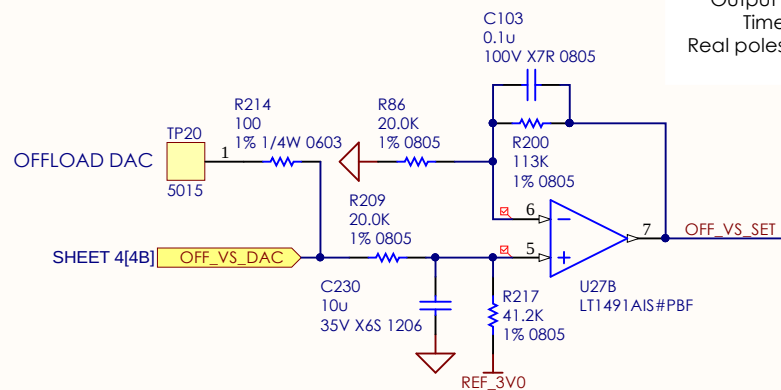
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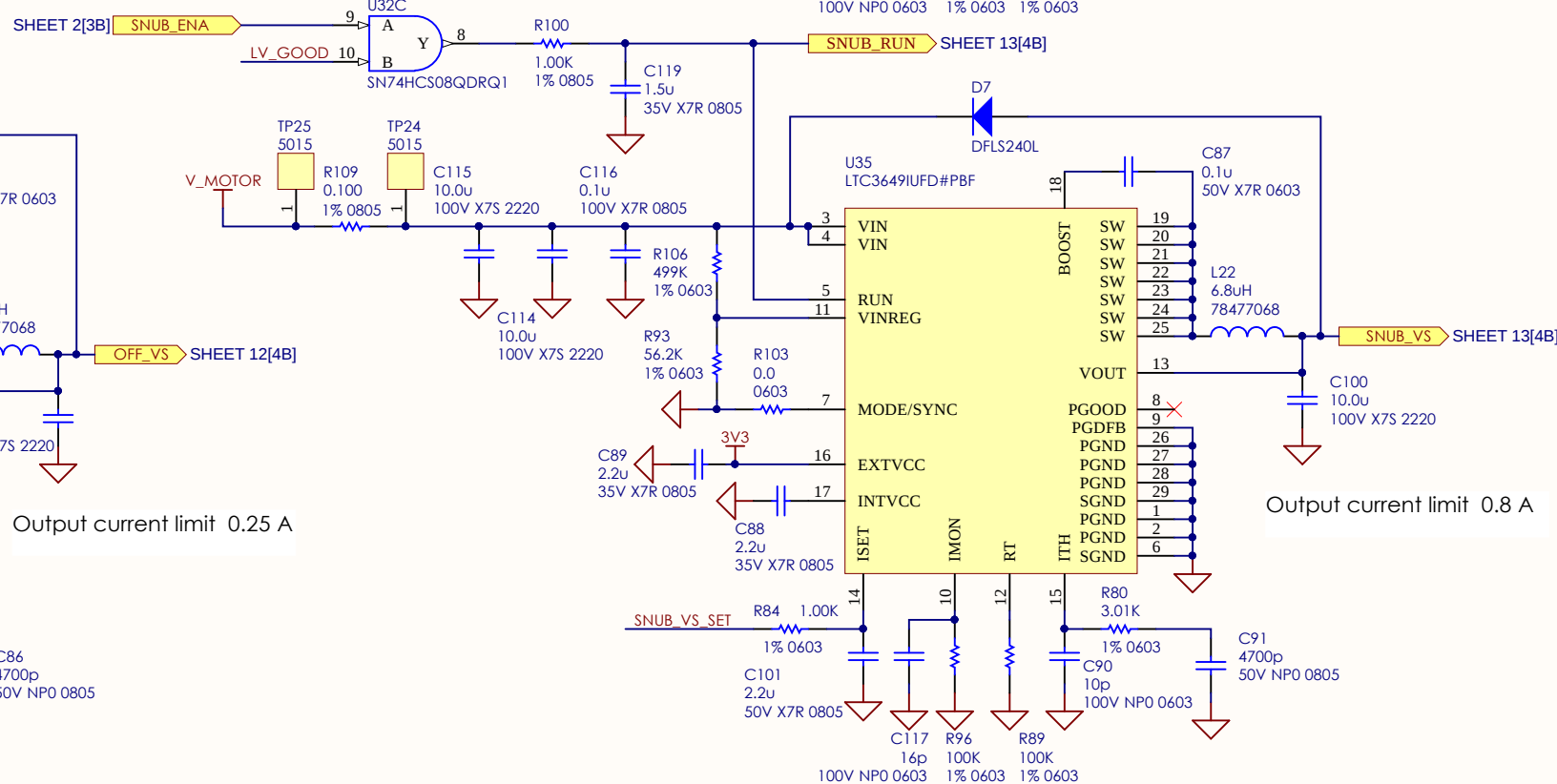
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12-bit DAC 0 to 3.0 V
Counts 0 to 4095
Output voltage 6.5 to 20 V
Time constant 0.14s
Real poles at 1.2Hz, 14Hz, 160Hz



Output current limit 0.8 A



Output current limit 0.8 A

Variable Power Supplies

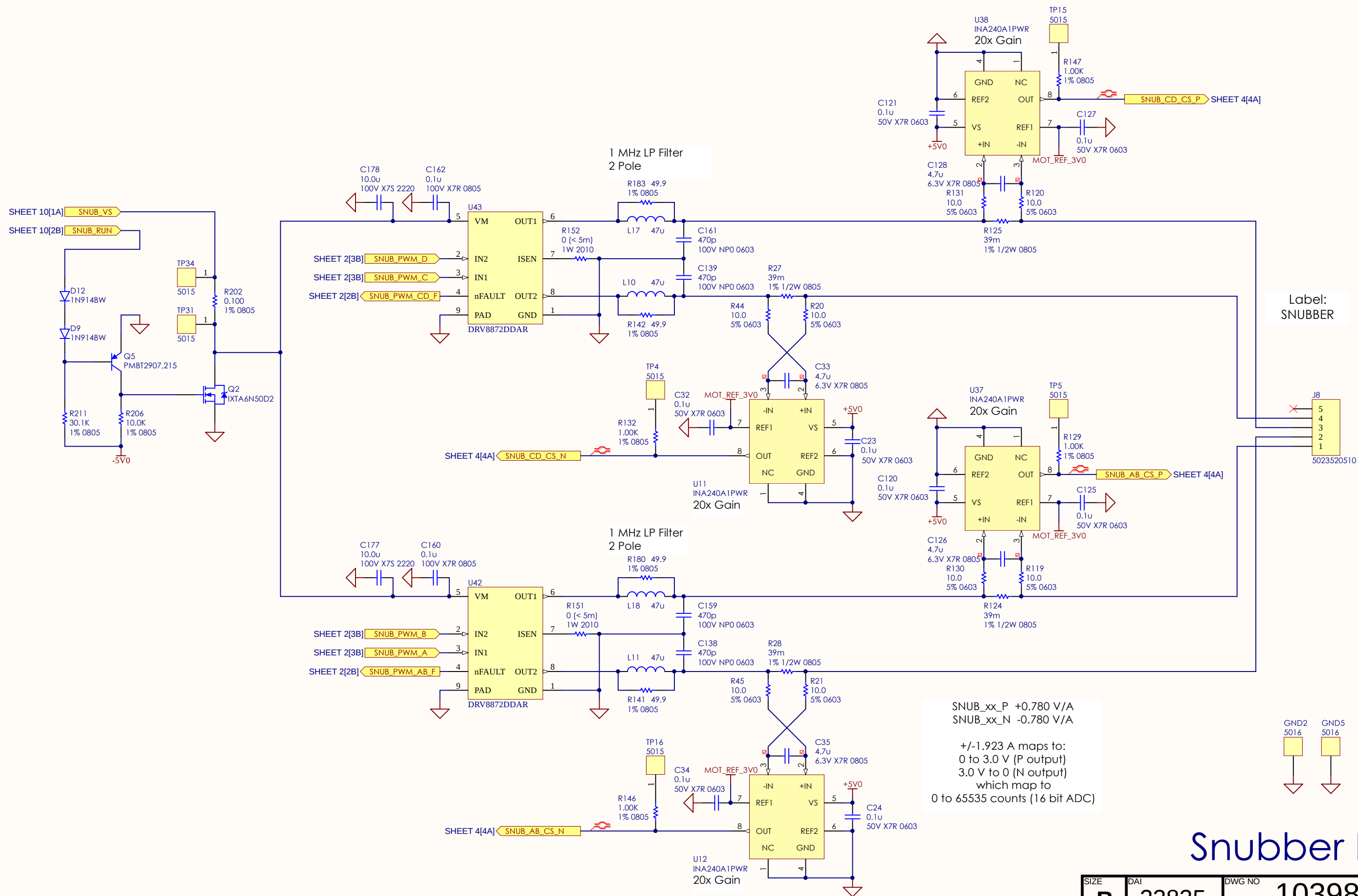
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REV 03/2020